Beyond Programmable Shading 2011

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Welcome

- 4\textsuperscript{th} consecutive year of Beyond Programmable Shading SIGGRAPH course

- This field changes *fast*
  - We re-write the content of this course every year
Key Events in Course History

• **2008:**
  – OpenCL and ComputeShader public sneak peek

• **2009:**
  – GPU architecture details explained, revealed and compared
  – Tiled deferred rendering in ComputeShader DX11

• **2010:**
  – Details of GPU 3D pipeline scheduling revealed
University Curriculum

• Stanford graduate course
  – Spring 2010 and spring 2011 (thanks Pat Hanrahan)
  – http://graphics.stanford.edu/wikis/cs448s-10
  – http://graphics.stanford.edu/wikis/cs448s-11

• University of Washington graduate course
  – Winter 2011 (thanks Brian Curless and Zoran Popovic)
Beyond Programmable Shading 2011
Interactive rendering techniques are created using an inseparable mix of data- and task-parallel algorithms and graphics pipelines.
The Wheel of Reincarnation

Gradually the processor became more complex.... Finally the display processor came to resemble a full-fledged computer with some special graphics features. And then a strange thing happened. We felt compelled to add to the processor a second, subsidiary processor, which, itself, began to grow in complexity. It was then that we discovered a disturbing truth. Designing a display processor can become a never-ending cyclical process. In fact, we found the process so frustrating that we have come to call it the "wheel of reincarnation."

(From BPS 2010)

Will There Be Another Turn of The Wheel of Reincarnation?

• Is “the rise of SW graphics” a temporary (5-10) year window as we go around the wheel of reincarnation or has the wheel stopped turning?

• If it has stopped turning, why?

• If it hasn’t stopped turning, what will be the next fixed-function hardware?
This Field Moves Fast

• Parallel computing *is* part of real-time rendering programming
  – E.g., tiled deferred rendering in ComputeShader

• But, real-time rendering platform is changing
Low Power
System on a Chip (SOC)

Tegra 2 – Heterogeneous Multi-core
Directions in BPS 2011

- Power
- System-on-a-chip (SOC) architectures
- Software rendering on GPUs and CPUs
- State-of-the-art of key rendering research
Beyond Programmable Shading I

9:00–9:20 – Aaron Lefohn, Intel
Why and How is Interactive Rendering Changing

9:20–9:45 – Peter-Pike Sloan, Disney
Research in Games

9:45–10:15 – Raja Koduri, Apple
The “Power” of Real-Time Rendering

10:15–10:45 – Mike Houston, AMD
Real-Time Rendering Architecture

Scheduling the Graphics Pipeline

11:15–11:35 - Aaron Lefohn, Intel
Parallel Programming for Real-Time Graphics

11:35–11:45 – Matt Pharr, Intel
High Performance Graphics on the CPU with ISPC

11:45–12:15 – Samuli Laine, NVIDIA
Jacopo Pantaleoni, NVIDIA
Software Rasterization on GPUs
Beyond Programmable Shading II

2:00–2:05 – Mike Houston, AMD
Welcome and Re-Introduction

2:05–2:45 – Jacob Munkberg, Intel
Toward a Blurry Rasterizer (State of the art)

2:45–3:15 – Marco Salvi, Intel
Order-independent Transparency (State of the Art)

3:15–3:45 – Chris Wyman, University of Iowa
Interactive Global Illumination (State of the art)

3:45–4:15 – Steve Parker, NVIDIA
User-Defined Pipelines for Ray Tracing
Beyond Programmable Shading II

4:15–5:15

Panel: *What is the Right Cross-Platform Abstraction for Real-Time 3D Rendering?*

Moderator: Peter-Pike Sloan
Disney Interactive

Panelists:
Raja Koduri, Apple
Chas Boyd, Microsoft
David Blythe, Intel
Mike Houston, AMD
Henry Moreton, NVIDIA
Course webpage and slides: http://bps11.idav.ucdavis.edu